AMENDMENTS TO THE SPECIFICATION:

Please amend Page 2, line 22-Page 3, line 4 to read as follows:

--For fiberoptic applications, SiGe/Si heterojunction diodes are a good choice for demodulating 1.3-1.6 ~~um~~ μm light at 300K. The use of 30% to 50% Ge is suggested to achieve absorption at the desired 1.3-1.6 ~~um~~ μm wavelength and low defects such as dislocations in the SiGe layer is needed to enhance the photodetector sensitivity. The state-of-the-art technology to achieve SiGe/Si heterojunction diodes with higher responsivity, low noise, and fast response is to form a 100-period SiGe/Si strained layer superlattice. However, the SiGe alloy ~~then~~ no longer behaves like the bulk material due to the quantum size effect. The net result of the quantum size effect is that the absorption occurs at wavelengths (1.1-1.3 ~~um~~ μm) shorter than expected. Therefore, a bulk SiGe alloy with desirable Ge content and low defects is needed to fabricate photodetectors that would absorb lights in the range of 1.3-1.6~~um~~ μm.--

Please amend Page 5, line 21-Page 6, line 12 to read as follows:

Epitaxial layer 30 is comprised substantially or completely of relaxed $Si_{1-y}Ge_y$ formed on upper surface 22 of layer 20. Layer 30 may have a thickness in the range from 200nm to 1000nm. The Ge content y in layer 30 is chosen to match the crystal lattice constant of upper surface 22 of layer 20 such that layer 30 is relaxed or essentially strain free. The Ge content y in layer 30 may be equal to or about the value of x at upper surface 22. The value y may be in the range from about 0.2 to about 0.5. An encapsulation layer 40 may be formed over the relaxed layer 30. Encapsulation layer 30 may be formed on upper surface 32 of layer 30 via PECVD, LPCVD, UHV CVD or spin-on techniques. Encapsulation layer 40 may have an upper surface

42. The encapsulation material may be, for example, Si, SiO_2, Poly Si, Si_3N_4, low-k dielectric materials, for example, Diamond Like Carbon (DLC), Fluorinated Diamond Like Carbon (FDLC), a polymer of Si, C, O, and H or a combination of any two or more of the foregoing materials. One example of a polymer of Si, C, O, and H is SiCOH which is described in U.S. Patent No. 6,147,009 to Grill, et al. ~~Serial no. 09/107567 filed Jun. 29, 1998 by Grill et al. entitled "Hydrogenated Oxidized Silicon Carbon Material" (Docket YOR919980245US1)~~ which is incorporated herein by reference. The deposition temperature for forming layer 40 may be below 900°C. The thickness of the encapsulation layer is in the range from 5nm to about 500nm. Encapsulation layer 40 functions to protect upper surface 32 of layer 30 or to provide an isolation layer.--

Please amend Page 6, line 22-Page 7, line 8 to read as follows:

--For a further description on polishing to reduce surface roughness, reference is made to Serial No. 09/675841 filed Sept. 29, 2000 by D.F. Canaperi et al. entitled "A Method of Wafer Smoothing for Bonding Using Chemo-Mechanical Polishing (CMP)" ~~(Docket YOR920000683US1)~~ which is incorporated herein by reference.

For a further description on bonding wafers to provide a bonded structure, reference is made to Serial No. 09/675840 filed Sept. 29, 2000 by D.F. Canaperi et al. entitled "Preparation of Strained Si/SiGe on Insulator by Hydrogen Induced Layer Transfer Technique" ~~(Docket YOR920000345US1)~~ which is incorporated herein by reference. The method of making SGOI by wafer bonding and H-implantation induced layer transfer is described in Serial No. 09/675840. This method can produce SiGe with higher Ge content onto an insulator compared

~~tot he~~ to the prior art. Further, this method can reduce the amount of defects in th SiGe layer due to the elimination of the misfit dislocations compared to the prior art. However, with this method, the transferred SiGe layer is relatively thin (<1 ~~um~~ μm) and transferring a high Ge content layer is still difficult to achieve due to implantation of H and annealing at 500 to 600°C to induce layer transfer.--

Please amend Page 7, lines 18-21 to read as follows:

--Fig. 3 shows the removal of the majority of the first substrate 10 which is in the range from about 600~~um~~ μm to about 750~~um~~ μm in thickness with a grinding or combination of grinding and polishing process. The remaining layer 70 of the first substrate 10 has a thickness in the range from about 50~~um~~ μm to about 100~~um~~ μm.--

Please amend Page 8, lines 10-16 to read as follows:

--Fig. 5 shows the cross-section view of a SiGe layer on insulator or a SiGe/Si ~~heterostreuture~~ heterostructure after applying a CMP process step to remove the step-graded $Si_{1-x}Ge_x$ layer 20. The structure has relaxed $Si_{1-y}Ge_y$ layer 30 on top. The chemical-mechanical planarization (CMP) process is used to remove the graded $Si_{1-x}Ge_x$ layer 20 and to adjust the thickness of the transferred relaxed $Si_{1-y}Ge_y$ layer 30. A final touch polishing and cleaning is used to smooth and clean the surface for epitaxial growth of strained Si/SiGe or for the deposition of a layer of n^+ Si as needed for forming a p-i-n photodetector.--